

```
mux 4 to 1 (input a, b, c, d, s, output f);  
  wire [0:3] x;  
  assign x = {a, b, c, d};  
  f = x[s];  
endmodule
```

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w_1	w_2	f
0	0	0
0	1	1
1	0	1
1	1	0

$$f(w_1, w_2)$$

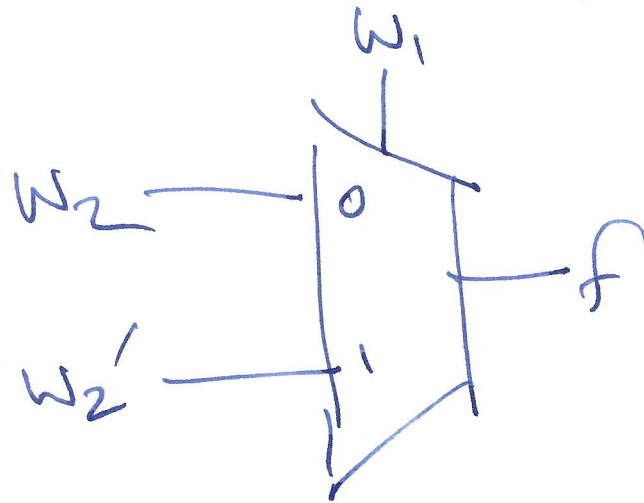
$$f = w_1' w_2 + w_1 w_2'$$

$$f = w_1' f_{w_1'} + w_1 f_{w_1}$$

$$f_{w_1'} = f(0, w_2)$$

$$= w_2$$

$$f_{w_1} = w_2'$$

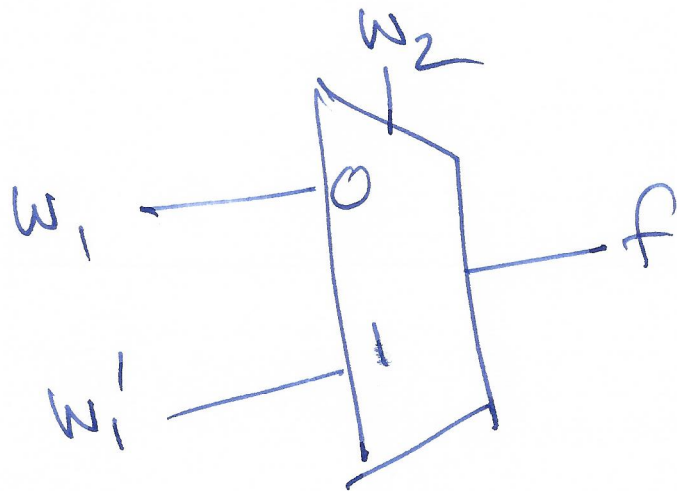


$$f(w_1, w_2) = w_1' w_2 + w_1 w_2'$$

$$f' = w_2' f_{w_2'} + w_2 f_{w_2}$$

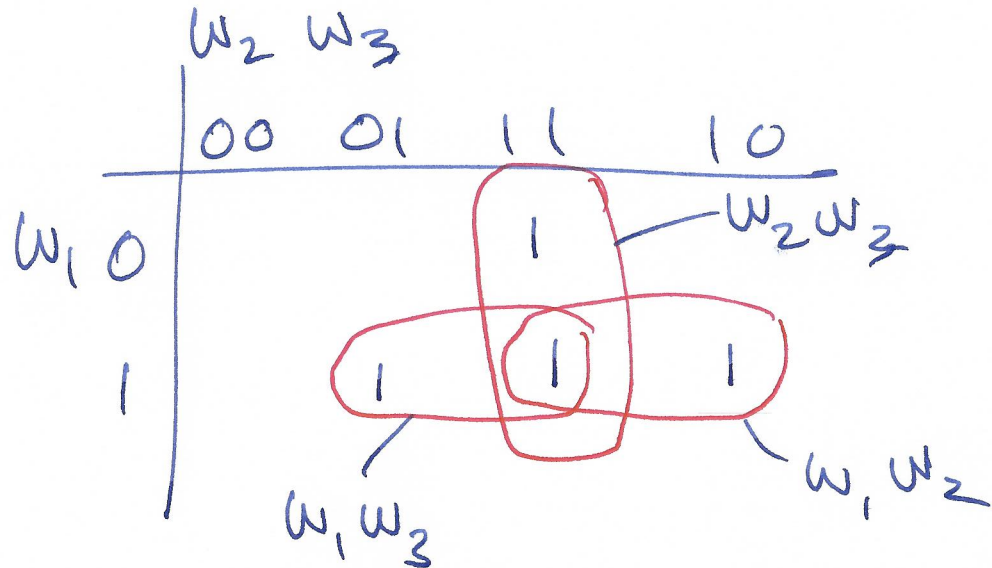
$$f_{w_2'} = f(w_1, 0) \quad f_{w_2} = f(w_1, 1)$$

$$f_{w_2'} = w_1 \quad f_{w_2} = w_1'$$



w_1	w_2	w_3	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$f = w_1 w_3 + w_1 w_2 + w_2 w_3$$



$$f_{w_1'} = w_2 w_3$$

$$f_{w_1' w_2'} = 0$$

$$f_{w_1' w_2} = w_3$$

$$f_{w_1} = w_3 + w_2 + w_2 w_3$$

$$f_{w_1 w_2'} = w_3$$

$$f_{w_1 w_2} = \cancel{w_3} \cdot 1$$

$$f = w_1 w_3 + w_1 w_2 + w_2 w_3$$

$$f_{w_1'} = w_2 w_3$$

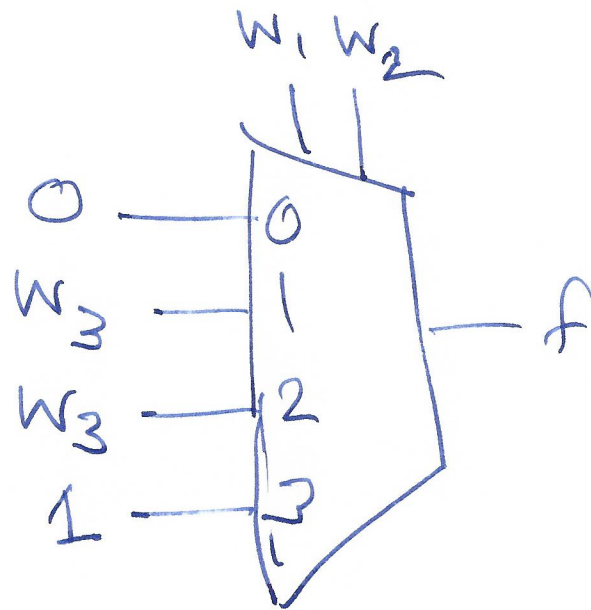
$$f_{w_1} = w_3 + w_2 + w_2 w_3$$

$$(00) f_{w_1' w_2'} = 0$$

$$(10) f_{w_1 w_2'} = w_3$$

$$(01) f_{w_1' w_2} = w_3$$

$$(11) f_{w_1 w_2} = 1$$



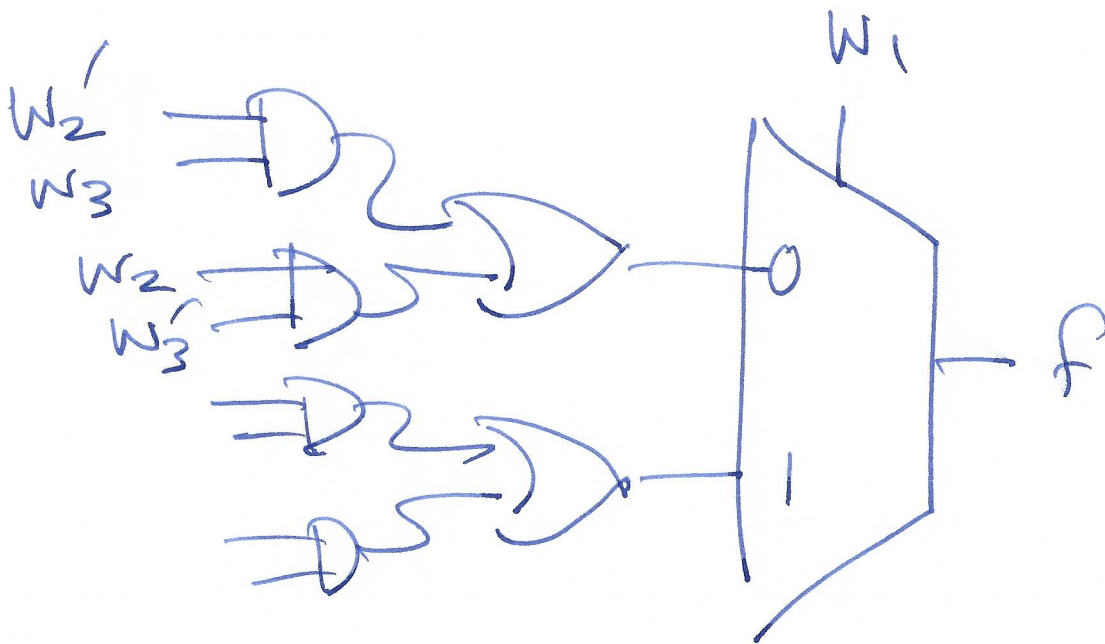
w_1	w_2	w_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

		$w_2 w_3$			
		00	01	11	10
w_1	0		1		1
	1	1		1	

$$f = w_1 w_2' w_3' + w_1' w_2' w_3 + w_1 w_2 w_3 + w_1' w_2 w_3'$$

$$f = W_1 W_2' W_3' + W_1' W_2' W_3 + W_1 W_2 W_3 + W_1' W_2 W_3'$$

$$f_{W_1'} = W_2' W_3 + W_2 W_3' \quad f_{W_1} = W_2' W_3' + W_2 W_3$$



$$f = w_1 w_2' w_3' + w_1' w_2' w_3 + w_1 w_2 w_3 + w_1' w_2 w_3'$$

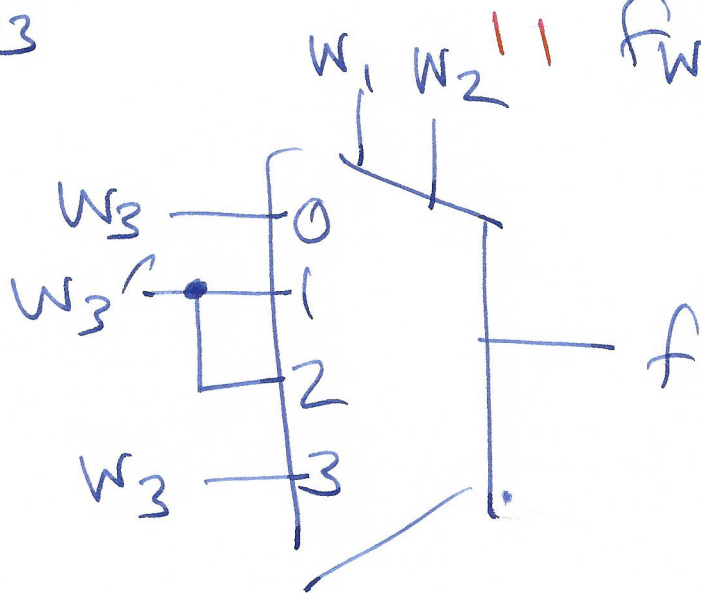
$$f_{w_1'} = w_2' w_3 + w_2 w_3' \quad f_{w_1} = w_2' w_3' + w_2 w_3$$

$$00 \quad f_{w_1' w_2'} = w_3$$

$$10 \quad f_{w_1 w_2'} = w_3'$$

$$01 \quad f_{w_1' w_2} = w_3'$$

$$11 \quad f_{w_1 w_2} = w_3$$



module Decode4to16 (input [3:0] s,
 input enable, output reg [0:15] f);

